Integrating Exact Simulation into Sweeping for Datapath Combinational Equivalence Checking

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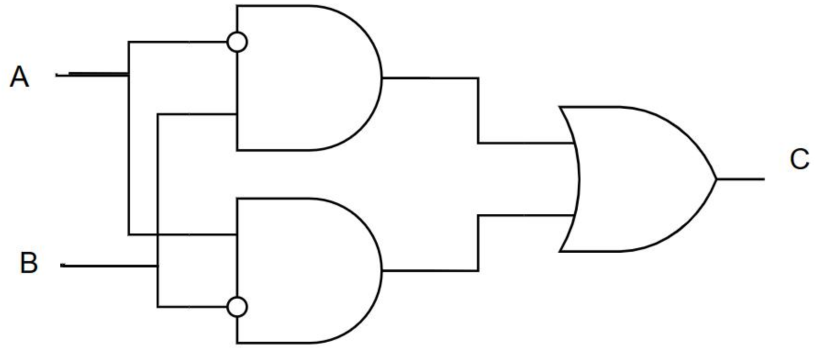
Outlin

- **Background and Related Works**
- Methods
  - Motivating Example
  - Main Framework
  - Improved Exact Simulation
  - Engine Selection Heuristic
  - Identical Structure Detection
- Experiments
- Conclusions

Combinational Equivalence Checking

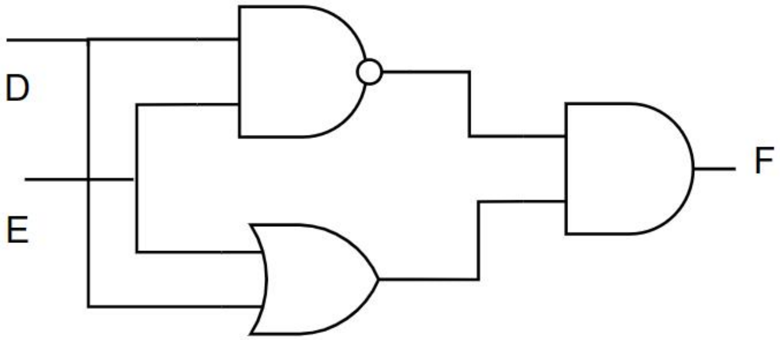
Circuit 1： $C = \bar{A}B +$



Truth Table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

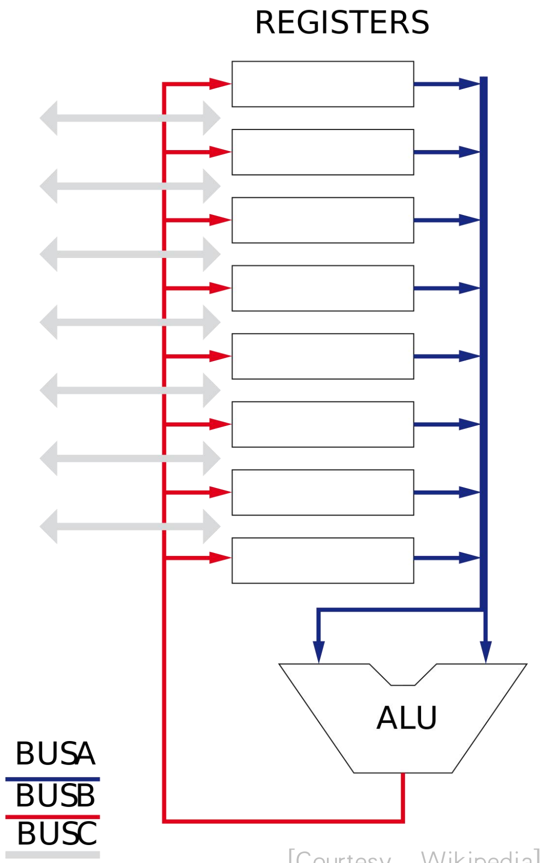
Circuit 2： $C = (\bar{A} + \bar{B})(A + B)$



Truth Table

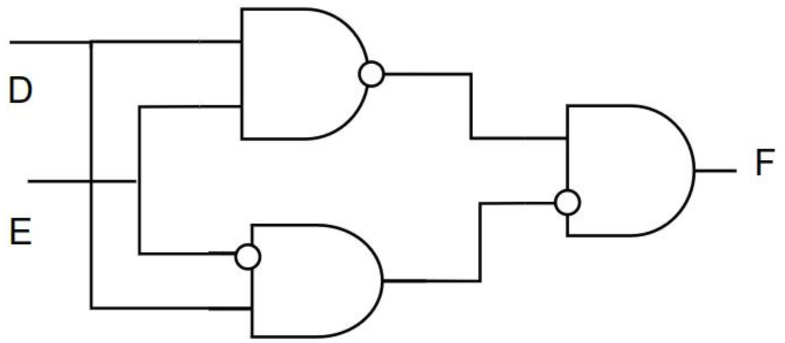
D	E	F
0	0	0
0	1	1
1	0	1
1	1	0

Backgroun Datapath Circuits & AIG & Miter

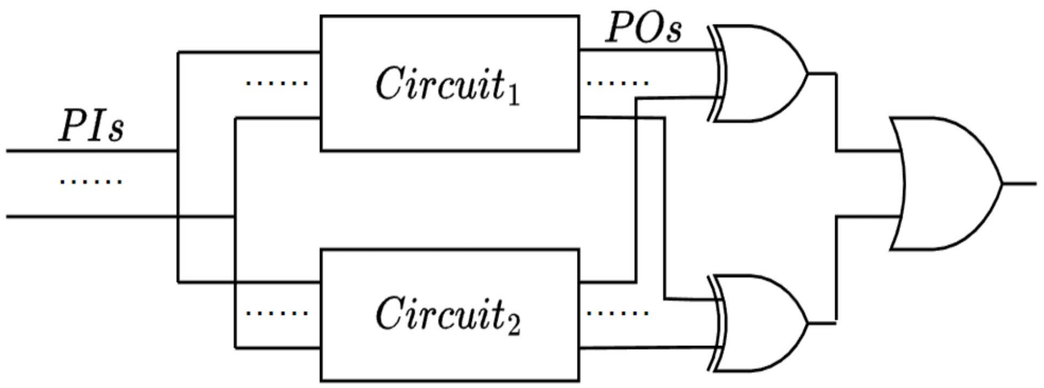


[Courtesy Wikipedia]

Datapath Circuit
with many XOR chains

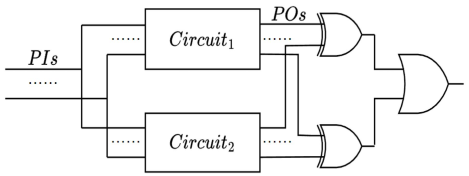


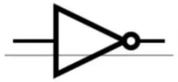
And Inverter Graph(AIG)



Miter Circuit

Background　Reasoning tools



Type	Operation	CNF Sub-expression
 AND	$C = A \cdot B$	$(\overline{A} \vee \overline{B} \vee C) \wedge (A \vee \overline{C}) \wedge (B \vee \overline{C})$
 NAND	$C = \overline{A \cdot B}$	$(\overline{A} \vee \overline{B} \vee \overline{C}) \wedge (A \vee C) \wedge (B \vee C)$
 OR	$C = A + B$	$(A \vee B \vee \overline{C}) \wedge (\overline{A} \vee C) \wedge (\overline{B} \vee C)$
 NOR	$C = \overline{A + B}$	$(A \vee B \vee C) \wedge (\overline{A} \vee \overline{C}) \wedge (\overline{B} \vee \overline{C})$
 NOT	$C = \overline{A}$	$(\overline{A} \vee \overline{C}) \wedge (A \vee C)$
 XOR	$C = A \oplus B$	$(\overline{A} \vee \overline{B} \vee \overline{C}) \wedge (A \vee B \vee \overline{C}) \wedge (A \vee \overline{B} \vee C) \wedge (\overline{A} \vee B \vee C)$

```
p cnf 20691 48881
227 226 225 224 223 222 221 220 219 218 2
158 135 -25 42 65 -78 -97  0
25 -158  0
-42 -158  0
-65 -158  0
78 -158  0
97 -158  0
171 25 -42 65 78 97 136  0
-25 -171  0
42 -171  0
-65 -171  0
-78 -171  0
-97 -171  0
190 137 25 -65 78 -97  0
-25 -190  0
65 -190  0
-78 -190  0
97 -190  0
198 137 25 42 -78 -97  0
-25 -198  0
-42 -198  0
78 -198  0
```

Miter Circuit
AIG

Tseitin Transformation

Boolean Formula
Conjunctive Normal Form (CNF)

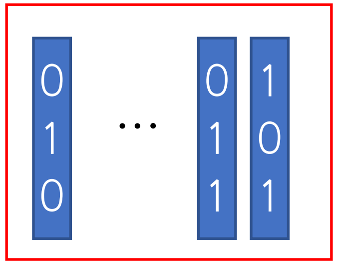
SAT solver
The Satisfiability Problem

BDD solver
The Binary Decision Diagram

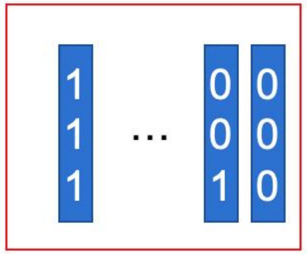
EPS Tool
Exact probability—based simulation

Background   Simulation & EPS

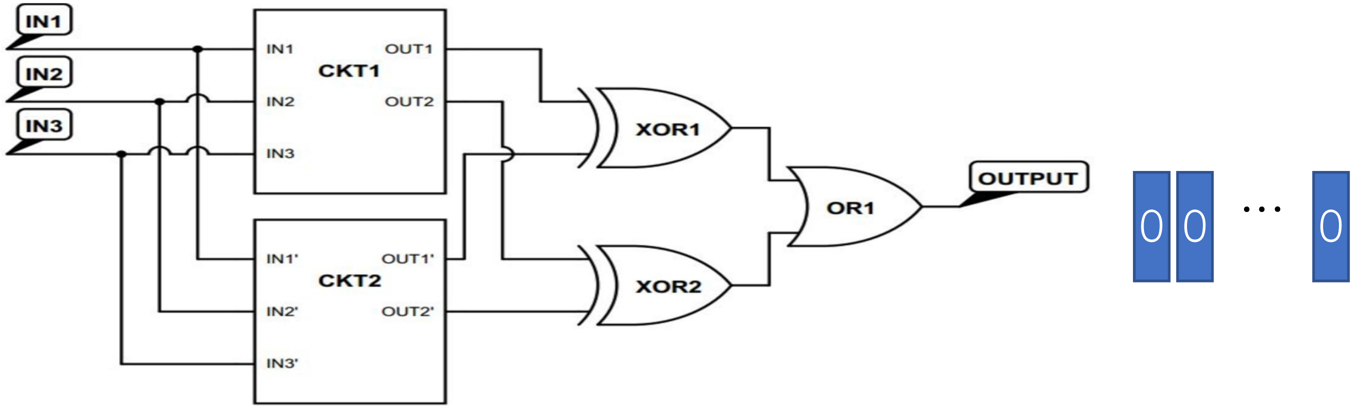
- **Logic Simulation & Exhaustive Search**



Logic Simulation



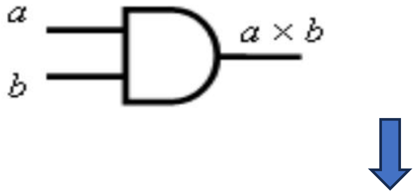
Exhaustive Search



- **EPS（Shih-Chieh Wu，et al. ATS 2006）**

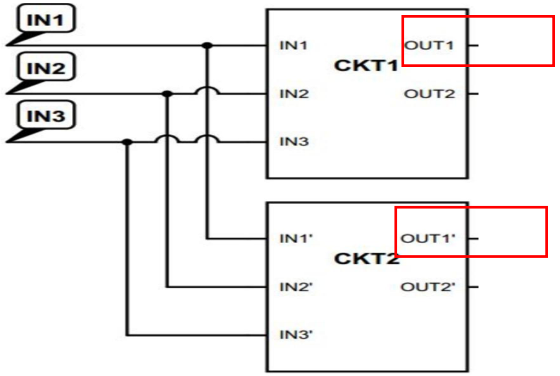
the probability for the i − th *PI should be assigned to 1/*θ_i

$\theta_1 = 3$ $\theta_{i+1} \leftarrow (\theta_i - 1)^2 + 1, i \in [1, N-1];$



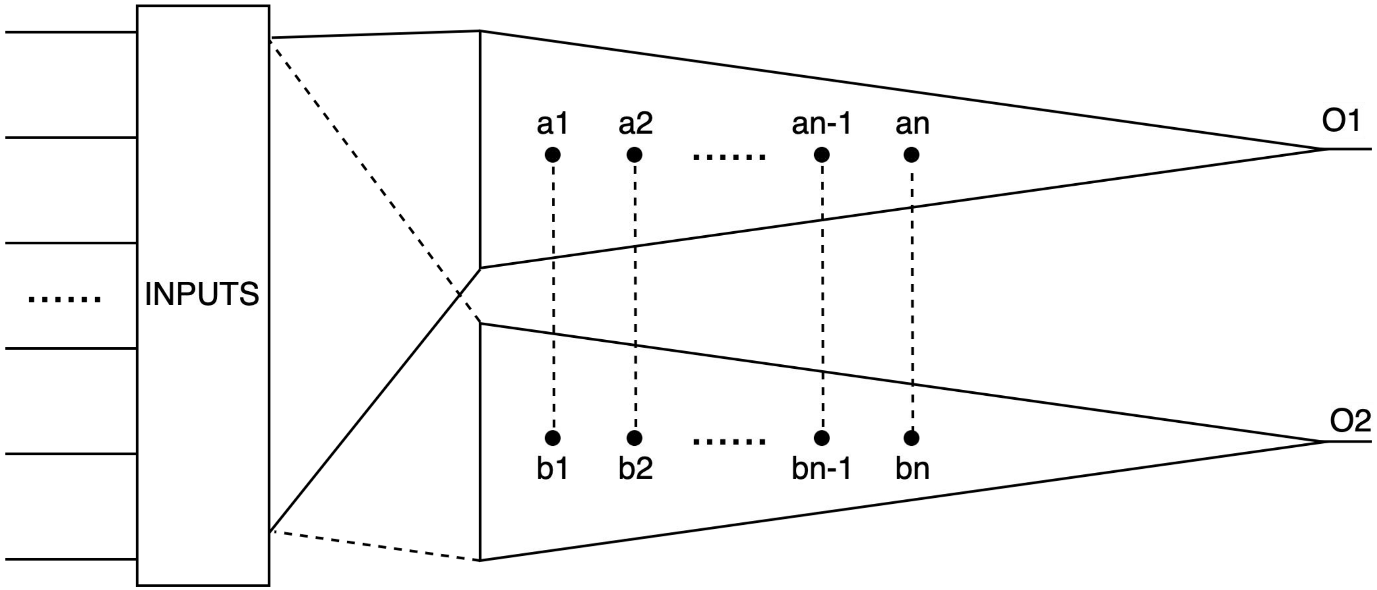
bitwise—AND（∩）   bitwise—INV

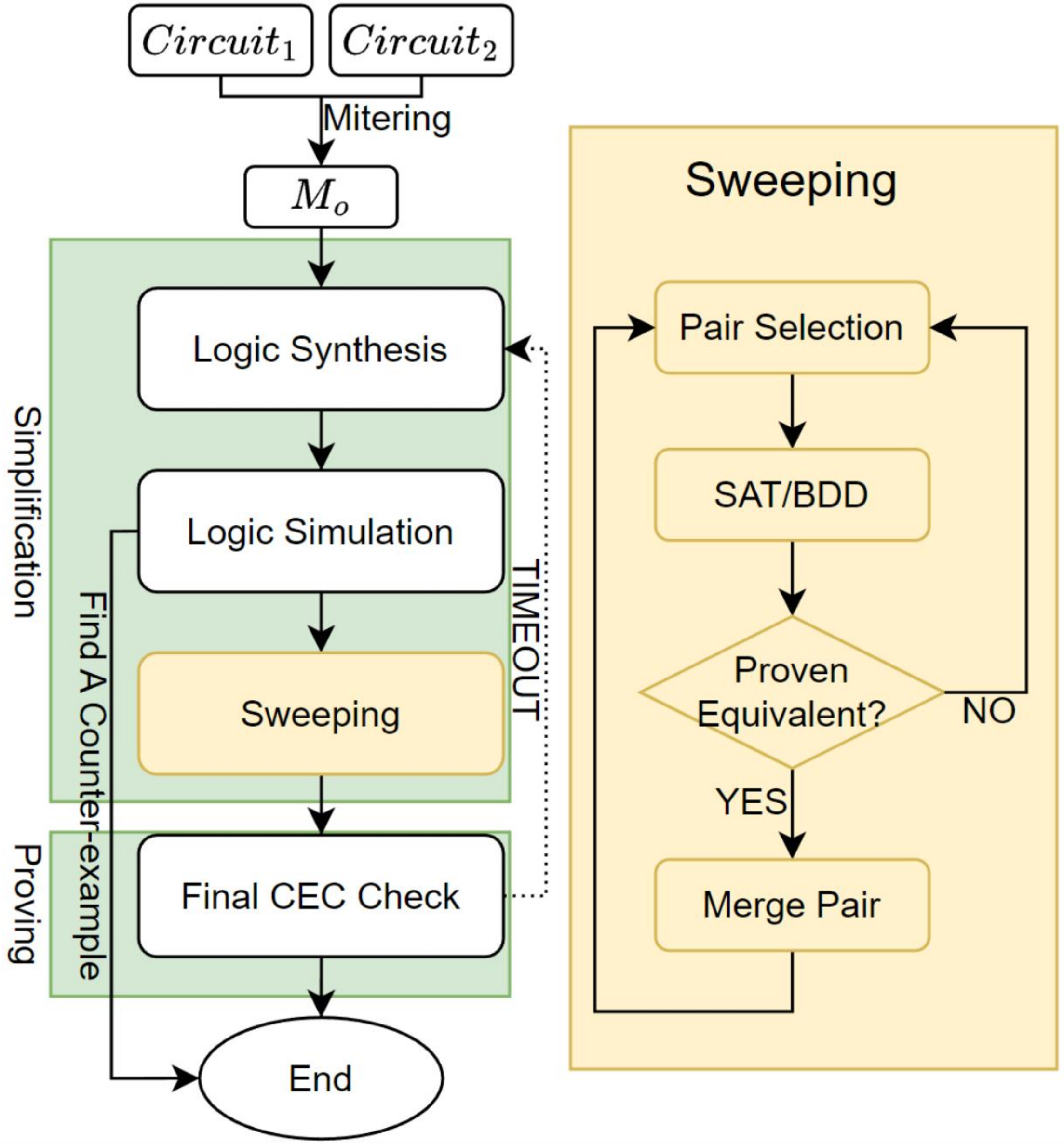
1/3
1/5
1/17



Compare the number of pairwise output

SAT/BDD – Sweeping Flow





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- Background and Related Works
- **Methods**
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  - **Main Framework**
  - **Improved Exact Simulation**
  - **Engine Selection Heuristic**
  - **Identical Structure Detection**
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Motivating Example

- **ec_h1**: an industrial instance from designing long bit-wise arithmetic circuits.
- ABC &cec cannot solve this instance.

- 2^{20} rounds logic simulation randomly.
- 113 potential-equivalent node pairs.
- 48 different structure

- SAT solver kissat-MAB vs. EPS

SAT and EPS are complementary

ID	Gates	PIs	Reasoning Tools	
			SAT	EPS
17	268	32	**<0.01**	9.67
18	353	18	1.75	**<0.01**
19	360	36	**<0.01**	TO
20	452	20	5.47	**<0.01**
21	556	22	29.40	**0.02**
22	468	40	**<0.01**	TO
23	548	44	**<0.01**	TO
24	678	24	137.32	**0.08**
25	658	48	**<0.01**	TO
26	807	26	903.51	**0.65**
27	768	52	**<0.01**	TO
28	1097	30	TO	**13.30**
29	950	28	TO	**2.94**
30	1423	32	TO	**66.41**
31	1310	64	**<0.01**	TO
32	1022	60	**<0.01**	TO
33	896	56	**<0.01**	TO
34	1259	32	TO	**59.64**
35	2018	32	TO	**90.56**
36	1734	32	TO	**79.45**
37	1580	32	TO	**73.27**
38	1832	64	**<0.01**	TO
39	1580	64	**<0.01**	TO
40	1446	64	**<0.01**	TO
41	1168	64	**<0.01**	TO
42	2262	32	TO	**132.24**
43	2144	32	TO	**122.90**
44	1879	32	TO	**84.97**
45	2046	64	**<0.01**	TO
46	1942	64	**<0.01**	TO
47	1708	64	**<0.01**	TO
48	4280	96	**<0.01**	TO

Framework of hybridCEC

Logic Simulation

Potential—Equivalent Pairs

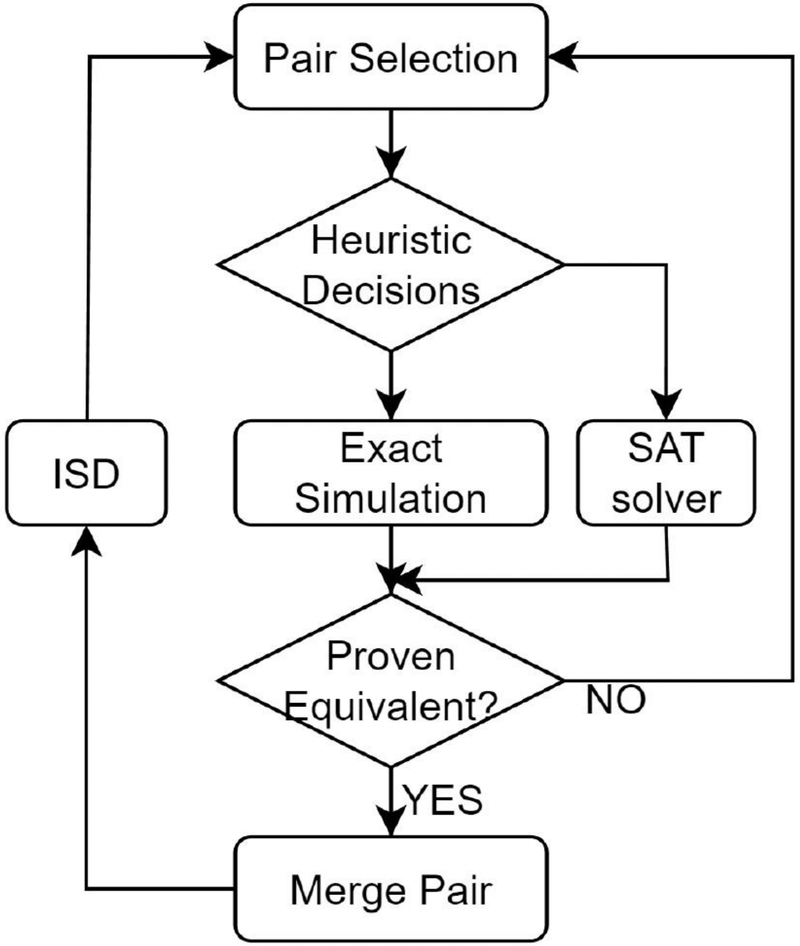


Fig. 4. Main Framework for Our CEC Algorithm.

Improved Exact Simulation

- EPS algorithm in assigns $1/\theta_i$ for the i-th PI. For a circuit with N PIs, the value i-th becomes a large integer $\theta_1\theta_2...\theta_N/\theta_i$ after reducing to a same denominator and eliminating the denominator.
- Each PI needs 2^N bits width because of the there are 2^N possible assignment patterns, which is memory costing.

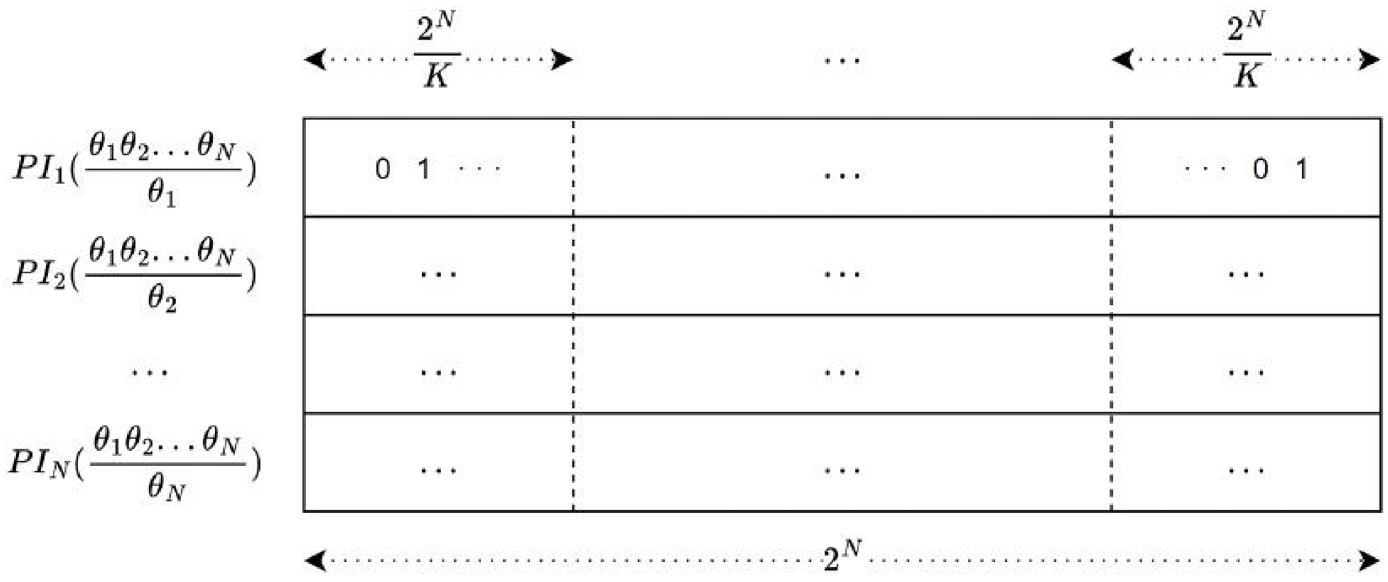


Fig. 5. Truncate the PI values into K blocks of small values.

Methods

Selection Heuristic

SAT V S **EPS**

SAT:

- Large but with simple structures
- Inefficient for circuits with many XOR chains
- Runtime can be considered as the time to refute XOR blocks

$$\sum_{b \in BS} 2^{|b|}$$

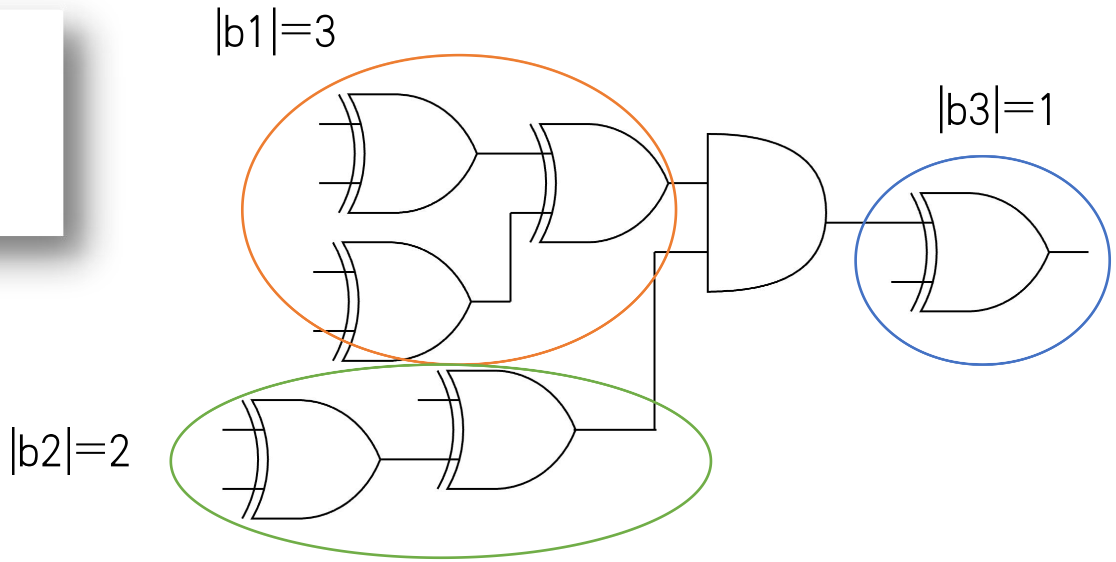
EPS:

- The runtime is determined by the number of PIs

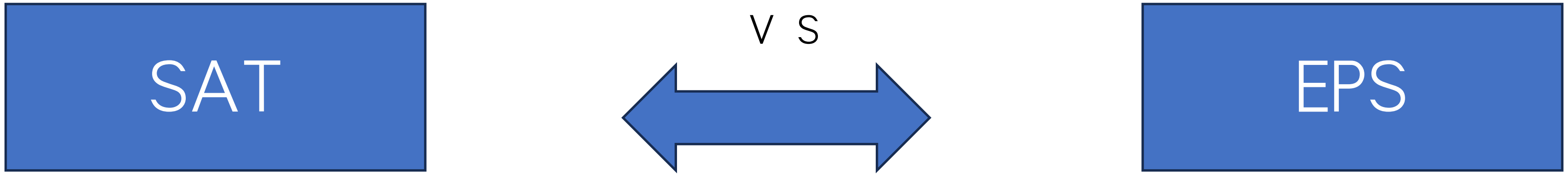
$$2^{|PI|}$$

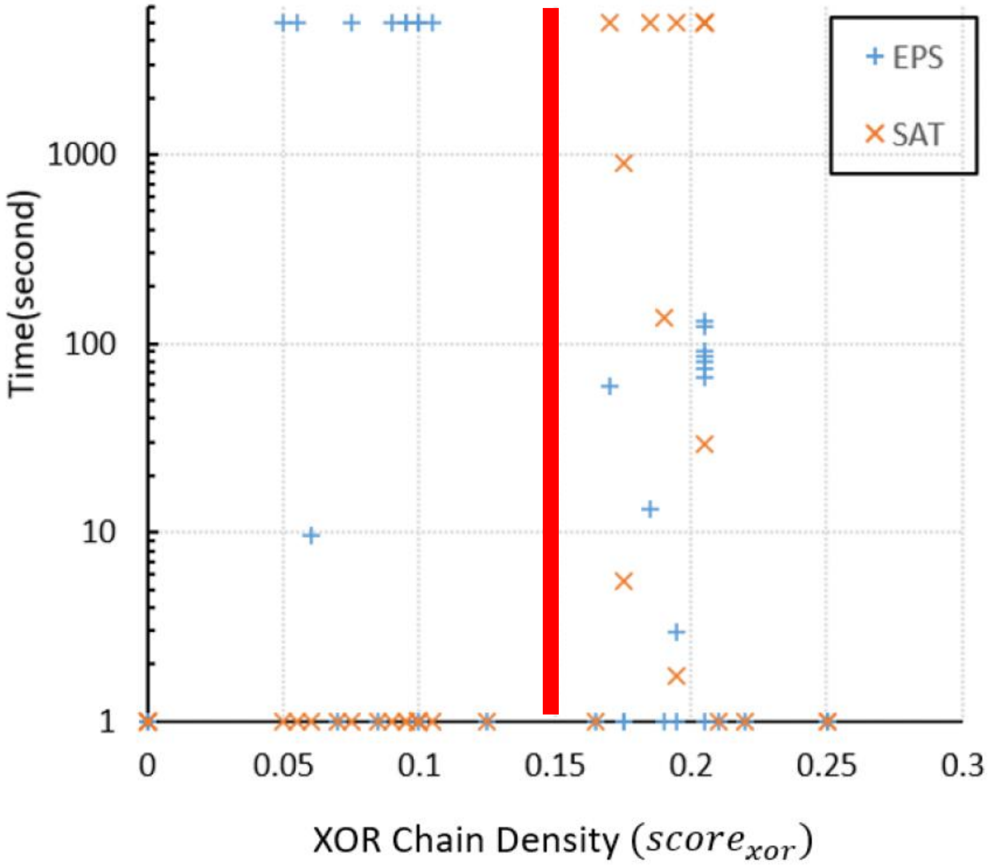
$$score_{XOR}(M) = log_2(\sum_{b \in BS} 2^{|b|})/N$$

- B is one XOR block
- BS is the set of XOR blocks
- N is the number of PIs



Selection Heuristic

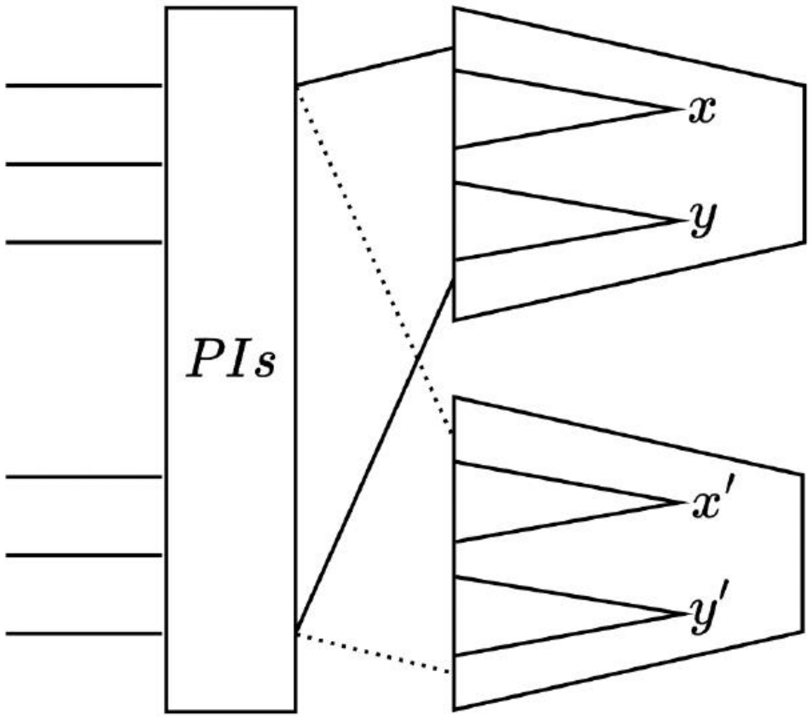




$$score_{XOR}(M) = log_2(\sum_{b \in BS} 2^{|b|})/N$$

Score > 0.15, pick EPS;
Score < 0.15, pick SAT

Methods — Identical Structure Detection (ISD)



Sweeping: SAT checking $x \leftrightarrow y$
SAT checking $x' \leftrightarrow y'$ (slow)

ISD: SAT checking $x \leftrightarrow y$
because $x \cong x', y \cong y'$ (fast!)
so $x' \leftrightarrow y'$

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Experimen Settings

- 50 industrial datapath circuits, which are AIG miters:
  - dp: datapath circuits with multiply-add hybrid arithmetic units
  - dpm: small datapath circuits with mainly multipliers
  - ec: mixed of dp and dpm.

- AMD EPYC 7763 CPU @ 2.45Ghz, 64 cores*2, 1T RAM, Ubuntu 20.04 LTS (64bit).

- CUTOFF = 3600s, 'TO' is stand for timeout

- Competitors of hybridCEC:
  - ABC &cec (state-of-the-art CEC SAT-sweeping tool)
  - Pure SAT (state-of-the-art SAT solver kissat-MAB)
  - Pure BDD (state-of-the-art BDD solver KCBOX)

Comparison with SOTA

Instance	Gates	Solver Name			
		HYBRIDCEC	ABC &cec	SAT	BDD
dpm_1_1	386	**0.01**	0.18	0.14	0.46
dpm_2_1	867	**0.02**	1.46	0.86	1.16
dpm_3_1	696	**0.01**	5.44	3.07	11.24
dpm_3_2	975	**0.02**	13.15	5.77	15.32
dpm_4_1	877	**0.02**	24.77	19.08	88.98
dpm_4_2	1333	**0.04**	60.11	21.97	81.06
dpm_4_3	1628	**0.08**	4.88	2.82	8.67
dpm_5_1	703	**0.01**	6.08	6.02	17.33
dpm_5_2	1319	**0.34**	1576.8	834.81	TO
dpm_5_3	2068	**0.84**	2198.41	491.28	2207.7
dpm_6_1	963	64.02	116.79	**57.55**	252.5
…	…	…			
ec_e1	280	**<0.01**	0.06	0.03	0.26
ec_e2	492	**0.01**	0.51	0.35	0.6
ec_m1	612	**<0.01**	0.04	0.1	0.53
ec_m2	1256	**0.02**	0.41	2.17	50.37
ec_m3	1664	**0.05**	2.55	12.54	1314.76
ec_h1	12499	**1464.17**	TO	TO	TO
ec_h2	13675	**3543.39**	TO	TO	TO
ec_h3	14152	TO	TO	TO	TO
ec_h4	15604	**2497.91**	TO	TO	TO
#Solved		**45**	25	26	23
#Best		**42**	1	3	0

Instance	Gates	Solver Name			
		HYBRIDCEC	ABC &cec	SAT	BDD
dp1_1	681	82.45	**13.93**	70.67	215.29
dp2_1	460	1.14	2.55	**0.59**	1.19
dp3_1	2116	**0.05**	10.98	218.8	TO
dp3_2	2647	**0.09**	TO	538.21	TO
dp3_3	7118	**25.7**	TO	TO	TO
dp3_4	8574	**47.98**	TO	TO	TO
dp3_5	10182	**42.63**	TO	TO	TO
dp4_1	1646	**0.05**	2.52	16.93	1951.42
dp4_2	5332	**24.32**	TO	TO	TO
dp4_3	10448	**171.28**	TO	TO	TO
dp4_4	11256	**267.02**	TO	TO	TO
dp4_5	12360	**487.97**	TO	TO	TO
dp5_1	18	**<0.01**	0.02	**<0.01**	0.18
dp5_2	1646	**0.03**	2.56	12.35	459.65
dp5_3	9798	**424.6**	TO	TO	TO
dp5_4	11484	**541.12**	TO	TO	TO
dp5_5	13617	**937.57**	TO	TO	TO
dp6_1	4585	**2.41**	TO	TO	TO
dp6_2	5332	**5.85**	TO	TO	TO
dp6_3	6128	**26.72**	TO	TO	TO
dp6_4	8690	**297.69**	TO	TO	TO
dp6_5	15787	TO	TO	TO	TO
dp7_1	1238	**0.03**	0.36	2.41	50.3
dp8_1	2116	**0.14**	10.11	104.41	2532.35
dp9_1	6128	**26.78**	TO	TO	TO
dp10_1	14049	TO	TO	TO	TO
dp11_1	20091	TO	TO	TO	TO
dp12_1	24773	TO	TO	TO	TO
dp13_1	378	**<0.01**	0.02	0.02	0.3
dp14_1	7061	**445.1**	TO	TO	TO

Behavior Analysis

Instance	Gates	Pairs	ISD	#SAT	T_{SAT}	#EPS	T_{EPS}
dpm_1_1	386	3	0	2	<0.01	1	<0.01
dpm_2_1	867	6	1	4	<0.01	1	<0.01
dpm_3_1	696	5	0	4	<0.01	1	<0.01
dpm_3_2	975	6	1	4	<0.01	1	<0.01
dpm_4_1	877	6	1	4	<0.01	1	0.02
dpm_4_2	1333	7	1	5	<0.01	1	0.03
dpm_4_3	1628	8	3	4	<0.01	1	0.05
dpm_5_1	703	5	0	4	<0.01	1	0.02
dpm_5_2	1319	9	4	4	<0.01	1	0.34
dpm_5_3	2068	13	7	5	<0.01	1	0.80
dpm_6_1	963	1	0	1	64.23	0	<0.01

… … …

ec_e1	280	3	0	2	<0.01	1	<0.01
ec_e2	492	3	0	2	<0.01	1	<0.01
ec_m1	612	20	10	8	0.01	2	<0.01
ec_m2	1256	30	16	10	<0.01	4	<0.01
ec_m3	1664	35	18	11	0.02	6	<0.01
ec_h1	12499	113	65	28	0.06	20	1465.44
ec_h2	13675	129	76	31	0.07	22	3548.04
ec_h4	15604	163	98	38	0.14	27	2497.60

Instance	Gates	Pairs	ISD	#SAT	T_{SAT}	#EPS	T_{EPS}
dp1_1	681	1	0	1	82.77	0	<0.01
dp2_1	460	1	0	1	1.13	0	<0.01
dp3_1	2116	40	22	12	0.01	6	<0.01
dp3_2	2647	45	25	13	0.02	7	0.02
dp3_3	7118	83	47	22	0.04	14	25.58
dp3_4	8574	101	59	25	0.06	17	47.81
dp3_5	10182	143	83	37	0.15	23	42.12
dp4_1	1646	35	19	11	0.01	5	<0.01
dp4_2	5332	65	37	17	0.02	11	24.16
dp4_3	10448	114	66	29	0.06	19	170.91
dp4_4	11256	127	75	31	0.21	21	266.83
dp4_5	12360	159	95	39	0.25	25	487.43
dp5_1	18	1	0	1	<0.01	0	<0.01
dp5_2	1646	35	19	11	0.01	5	<0.01
dp5_3	9798	98	57	24	0.16	17	424.23
dp5_4	11484	119	69	30	0.08	20	540.56
dp5_5	13617	171	100	44	43.60	27	893.61
dp6_1	4585	60	34	16	0.01	10	2.23
dp6_2	5332	65	37	17	0.02	11	5.73
dp6_3	6128	70	40	18	0.02	12	26.60
dp6_4	8690	85	48	22	0.04	15	297.50
dp7_1	1238	30	15	11	0.01	4	<0.01
dp8_1	2116	40	22	12	0.01	6	0.01
dp9_1	6128	70	40	18	0.02	12	26.64
dp13_1	378	15	7	6	<0.01	2	<0.01
dp14_1	7061	75	43	19	0.04	13	445.30

- The number of pairs (Pairs)
- The number of pairs reduced by ISD (ISD)
- The number of SAT calls (#SAT), EPS (#EPS), and the time used in SAT solver (T_{SAT}) and EPS (T_{EPS})

Experimen Strategy Assessments

Instance	Gates	Solver Name				
		HYBRIDCEC	V_1	V_2	V_3	V_4
dpm_1_1	386	**0.01**	0.12	0.02	0.03	**0.01**
dpm_2_1	867	**0.02**	0.89	0.17	0.07	**0.02**
dpm_3_1	696	**0.01**	2.82	0.08	0.04	**0.01**
dpm_3_2	975	0.02	5.55	0.13	0.07	**0.01**
dpm_4_1	877	**0.02**	23.42	0.2	0.14	0.03
dpm_4_2	1333	**0.04**	27.16	0.07	0.24	0.05
dpm_4_3	1628	**0.08**	2.9	0.12	0.28	0.09
dpm_5_1	703	**0.01**	6.43	0.06	0.11	0.03
dpm_5_2	1319	**0.34**	1334.05	5.04	3.85	0.96
dpm_5_3	2068	0.84	681.02	**0.31**	4.84	1.09
dpm_6_1	963	64.02	64.77	**0.79**	70.36	191.45
…	…	…				
ec_e1	280	**<0.01**	0.04	0.02	0.03	0.01
ec_e2	492	**0.01**	0.28	0.06	0.03	**0.01**
ec_m1	612	**<0.01**	0.02	29.89	0.05	0.01
ec_m2	1256	**0.02**	0.1	TO	0.1	0.05
ec_m3	1664	**0.05**	0.44	TO	0.19	**0.05**
ec_h1	12499	1464.17	TO	TO	TO	**1061.78**
ec_h2	13675	**3543.39**	TO	TO	TO	TO
ec_h3	14152	TO	TO	TO	TO	TO
ec_h4	15604	**2497.91**	TO	TO	TO	3161.23
#Solved		**45**	27	18	39	44
#Best		**35**	1	3	2	13

- V_1: using only SAT solver in sweeping.
- V_2: using only EPS to prove in sweeping.
- V_3: disable the ISD technique.

Instance	Gates	Solver Name				
		HYBRIDCEC	V_1	V_2	V_3	V_4
dp1_1	681	**82.45**	109.91	1469.39	89.57	307.97
dp2_1	460	1.14	1.15	10.27	**1.11**	2.51
dp3_1	2116	**0.05**	1.98	TO	0.22	0.13
dp3_2	2647	**0.09**	7.21	TO	0.35	0.2
dp3_3	7118	**25.7**	TO	TO	120.24	64.11
dp3_4	8574	**47.98**	TO	TO	233.99	98.52
dp3_5	10182	**42.63**	TO	TO	471.04	50.28
dp4_1	1646	**0.05**	0.53	TO	0.12	0.08
dp4_2	5332	24.32	TO	TO	103.58	**19.81**
dp4_3	10448	171.28	TO	TO	1271.06	**85.0**
dp4_4	11256	267.02	TO	TO	2500.96	**113.66**
dp4_5	12360	**487.97**	TO	TO	3387.28	879.55
dp5_1	18	**<0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**
dp5_2	1646	**0.03**	0.74	TO	0.15	0.11
dp5_3	9798	**424.6**	TO	TO	2813.27	1104.36
dp5_4	11484	**541.12**	TO	TO	TO	1535.88
dp5_5	13617	**937.57**	TO	TO	TO	2722.96
dp6_1	4585	**2.41**	1220.27	TO	27.9	3.14
dp6_2	5332	**5.85**	TO	TO	169.79	21.32
dp6_3	6128	**26.72**	TO	TO	588.2	232.32
dp6_4	8690	**297.69**	TO	TO	TO	1765.74
dp6_5	15787	TO	TO	TO	TO	TO
dp7_1	1238	**0.03**	0.2	TO	0.09	0.08
dp8_1	2116	**0.14**	2.0	TO	0.47	0.16
dp9_1	6128	26.78	TO	TO	889.63	**24.9**
dp10_1	14049	TO	TO	TO	TO	TO
dp11_1	20091	TO	TO	TO	TO	TO
dp12_1	24773	TO	TO	TO	TO	TO
dp13_1	378	**<0.01**	0.02	0.42	0.01	0.02
dp14_1	7061	445.1	TO	TO	3330.51	**157.6**

- V_4: replacing the SAT solver with MINISAT [26].

Conclusio

- A hybrid CEC algorithm called hybridCEC for Datapath circuits.
- In the future, we plan to develop a parallel version of hybridCEC.

Thank You!

Q&A